What is claimed is:

1. A method for referring to an address of vector data, the method being for referring to a memory address to read or write vector data with the use of an index vector, wherein

an element storage register for storing an element of the index vector is divided into multiple areas; a particular code is stored in each of the areas; and multiple index vectors may be generated with the use of the code stored in a particular area of each element storage register of the index vector.

2. The method for referring to an address of vector data according to claim 1, wherein

each area of the element storage register stores a code indicating a relative address to a reference base address of the index vector; and

a target address, a memory address to be referred to, is calculated based on the code in an area selected from the divided areas of each element storage register and the base address.

3. The method for referring to an address of vector data according to claim 2, wherein the index vector is stored in a vector register, and a code indicating the relative address is stored in each area obtained by dividing each element register of the vector register.

4. The method for referring to an address of vector data according to claim 1, wherein

each area of the element storage register stores a code indicating a relative address to a reference base address of the index vector; and

a target address, a memory address to be referred to, is calculated based on the code in an area selected from the divided areas of each element storage register and the base address, and the calculated target address is set as a new reference base address.

5. The method for referring to an address of vector data according to claim 4, wherein a code indicating the relative address is stored in a scalar register as the element storage register, and the code indicating the relative address is stored in each area of the scalar register.

6. The method for referring to an address of vector data according to any of claims 1 to 5, wherein the area to be selected from the divided areas is dynamically changed during execution of a vector instruction for reading or writing of the vector data.

7. The method for referring to an address of vector data according to claim 6, wherein a specification pattern for specifying the area to be selected from the divided areas of the element storage register is stored in a predetermined

register, and a particular index vector is generated by specifying any of the divided areas based on the specification pattern.

8. The method for referring to an address of vector data according to any of claims 1 to 7, wherein a first register including the element storage register storing a first index vector element and a second register including the element storage register storing a second index vector element are provided, and multiple index vectors may be generated with the use of the code stored in a particular area of each of the first and second registers.

9. A vector processor for referring to a memory address to read or write vector data with the use of an index vector, the vector processor comprising:

an element storage register for storing an element of an index vector; wherein

the element storage register is divided into multiple areas, and a particular code is stored in each of the areas; and

multiple index vectors may be generated with the use of the code stored in a particular area of each element storage register.

10. The vector processor according to claim 9, wherein a first register including the element storage register storing a first

index vector element and a second register including the element storage register storing a second index vector element are provided, and multiple index vectors may be generated with the use of the code stored in a particular area of each of the first and second registers.